Table of Contents

REVISIONS

REVISION	DESCRIPTION	DATE	APPROVED
-	Initial release	10/2/07	

GENERAL RELEASE DOCUMENT.
CONSULT FACTORY FOR CURRENT REVISION.

SPECIFICATION CONTROL DRAWING

PREPARED BY	DATE
E.Jackson	
CHECKED BY	DATE
B.Remtulla	
RELEASED BY	DATE
T.Mitchell	

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES:
3 PLACE DECIMAL = .005
2 PLACE DECIMAL = .02
1 PLACE DECIMAL = .1
FRACTIONS = ± 1/16
ANGLES = 2 DEGREES

Q-TECH CORPORATION
10150 W. JEFFERSON BLVD.
CULVER CITY, CA. 90232-3510

TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR, CLASS S, DETAIL SPECIFICATION FOR

DRAWING NO.	REV.
QT601S	**-**

SCALE:	SIZE	CAGE CODE	
NONE	**A**	**51774**	SHEET 1 of 5

1 SCOPE

1.1 Scope. This specification establishes the detail requirements for hybrid, hermetically sealed, CMOS output temperature compensated crystal oscillators for use in space flight missions.

1.2 Part number. The part number shall be as specified in Table I herein.

2 APPLICABLE DOCUMENTS

2.1 Specifications and standards. Unless otherwise specified, the following documents shall be applicable to this specification to the extent specified herein.

SPECIFICATIONS

401-0298-017 Hybrid Crystal Oscillators, TCXO, Class S, General Specification For

3 REQUIREMENTS

3.1 General requirements. The individual item requirements shall be as specified in the General Specification with the exceptions, modifications, and additions specified herein.

3.2 Design and construction

3.2.1. Outline dimensions and terminal connections. The outline dimensions and terminal connections shall be as shown in Figure 1 and 2 herein.

3.2.2. Package body and lead finish. The package body and lead finish shall be gold in accordance with MIL-PRF-38534.

3.2.3. Active Devices. For output frequencies greater than 10 MHZ, the CMOS micorcircuit used in this part shall be National Semiconductor Corporation (NSC) 54AC00 from a wafer proven to be radiation tolerant to 100 kRad (Si) total ionizing dose. This device is specified to be *single event latchup free* (see DSSC SMD 5962-87549) for LET up to 93 MeV-cm^2/mg. For lower frequencies the CMOS microcircuit shall be Intersil Corporation 54ACS family, Silicon on Sapphire technology, from a wafer proven to be radiation tolerant to 300 kRad (Si).

3.3 Performance requirements

3.3.1. Maximum ratings. The maximum ratings shall be as specified in Table II herein.

3.3.2. Electrical performance characteristics and limits. The electrical performance requirements and limits shall be in accordance with Table III.

3.3.3. Delta limits. Except for frequency aging (refer to Table III herein), delta limits shall be in accordance with the General Specification.

3.3.4. Total dose radiation limits. Hybrid crystal oscillators supplied in accordance with this specification shall be capable of meeting the performance requirements after being exposed to 100 krad total dose radiation levels.

4 QUALITY ASSURANCE PROVISIONS

4.1 General. The quality assurance provisions shall be in accordance with the General Specification with the exceptions, modifications, and additions specified herein.

4.2 Screening tests. The screening tests shall be in accordance with the General Specification.

4.2.1. Frequency-Temperature Stability (tolerance) test method. Devices shall be trimmed via adjustment of external resistor to ground, pin 1, for frequency accuracy at T = 25 ºC during pre Burn-in and Group A Electrical test (prior to temperature sweep). Value shall be recorded as part of the test data. Table III

limit applies only for these two electrical tests, but data shall be recorded for interim and final electrical using the resistor value obtained during pre Burn-in electrical test.

4.3 Quality Conformance Inspection. Quality Conformance Inspection shall be in accordance with the General Specification and as specified herein.

4.4 Frequency-Temperature Stability test method. Test limit shall apply with reference to room temperature only rather than nominal frequency for QCI Group C, subgroups 2 and 4. Test data shall be recorded with reference to nominal frequency, however, using the external trim resistor value as determined during Group A Electrical test (prior to temperature sweep), if available, or else the nominal value (5 kohms).

5 PACKAGING

5.1 Preservation, packaging and packing. Hybrid crystal oscillators shall be prepared for delivery in accordance with the General specification.

6 NOTES.

6.1 Notes. The notes of the General Specification are applicable to this drawing.

6.2 Ordering information. The procuring activity shall advise Q-Tech Corporation at the time of Request for Quotation if quality conformance inspection is to be required.

6.2.1. Part Number.

QT601S A B M - 16.00000 MHZ

Model #

Supply voltage: A: 5.0 volts; L: 3.3 volts

Temp stability - see Table I

Screening: E: engineering model; M: flight model

Frequency (7 digits)

TABLE I. STABILITY / TEMPERATURE OPTIONS

OPTION	TEMP STABILITY
A	± 2 PPM, -45 °C TO +85 °C
B	± 1 PPM, -40 °C TO + 80 °C
C	± 1 PPM, -40 °C TO + 70 °C
D	± 1 PPM, -20 °C TO + 70 °C
E	± 0.5 PPM, 0 °C TO +50 °C

TABLE II. MAXIMUM RATINGS

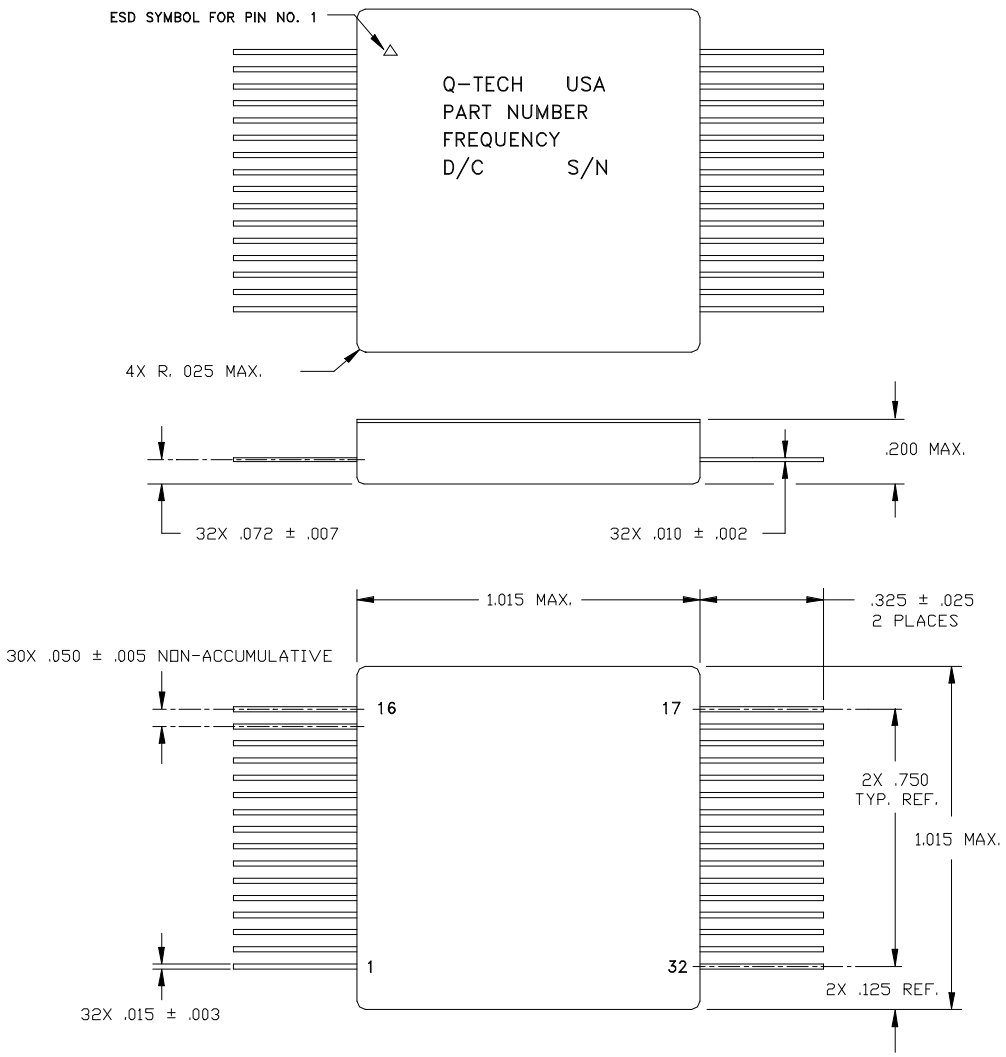
Parameter	Symbol	Min	Max	Units
Supply voltage, “A”	V_{CC}	0	5.65	Volts
Supply voltage, “L”	V_{CC}	0	5.25	Volts
Operating temperature	T_C	-55	125	ºC
Storage temperature	Tstg	-65	125	ºC
Lead solder temperature/time			250/10	ºC/seconds
Package thermal resistance	θjc		50	ºC/W

TABLE III. ELECTRICAL PERFORMANCE CHARACTERISTICS

ELECTRICAL PARAMETER	TEST CONDITIONS 3/,4/	LIMITS				NOTES
		MIN.	NOM.	MAX.	UNITS	
FREQUENCY RANGE		3 to 32 MHZ				
FREQUENCY/TEMPERATURE STABILITY		see Table I				1/, 2/
FREQUENCY/TEMPERATURE STABILITY, EXTENDED RANGE	-55 ºC, +90 ºC			± 30	ppm	
SUPPLY VOLTAGE (Vcc) TOLERANCE		-5%		+ 5%	%	
FREQUENCY VOLTAGE STABILITY	For ± 5% change in Vcc			± 0.2	ppm	
LOAD PULLING	±10 % change in load			± 0.2	ppm	
INPUT CURRENT	Frequency range, MHZ					
	Less than 10			20	mA	
	10 - 32			25	mA	
LOAD				15	pF	
OUTPUT VOLTAGE - LOGIC "0"				0.1xVcc	Vdc	5/
OUTPUT VOLTAGE - LOGIC "1"		0.9xVcc			Vdc	5/
RISE / FALL TIME				4	nsec	
DUTY CYCLE	Measured at Vcc/2	50 ± 10			%	
FREQUENCY AGING (AFTER 30 DAYS)	70 °C ± 2 °C			± 0.4	ppm	
FREQUENCY AGING (AFTER 5 YEARS)	70 °C ± 2 °C			± 4.0	ppm	6/
STARTUP TIME				10	ms	
PHASE NOISE	25 ºC,@ sideband freq (Hz): 10 100 1000 10000 100000			 -75 -105 -130 -140 -145	dBc	7/
FREQUENCY ADJUSTMENT RANGE			± 5		ppm	8/
FREQUENCY TRIM SENSIVITIY, EXTERNAL RESISTOR	Nominal value = 5 kohms		-1		ppb / ohm	9/
FREQUENCY TRIM SENSIVITIY, TUNING VOLTAGE	range: 0 - .5 volts		-20		ppm / volt	9/
VIBRATION SENSITIVITY	Δf/f per g, all 3 axes		10		ppb/g	10/

NOTES

1/ Frequency/Temperature Stability (tolerance) is referenced to nominal output frequency and includes trimming with a 1% external resistor to ground, pin 1. Required value shall be provided at the time of shipment.
2/ Shall be measured using continuous temperature ramp (slew) from -50 ºC to 90 ºC followed by a ramp from 90 ºC to -50 ºC with end point dwell no greater than 1 hour. Temperature rate shall be no greater than 0.5°C per minute with readings recorded in increments no greater than 0.3°C. Test data shall be plotted to show thermal hysteresis.
3/ Unless otherwise specified, the limits are over the full operating temperature range, under specified load conditions and nominal supply voltage.
4/ Unless otherwise specified, all measurements are in accordance with MIL-PRF-55310.
5/ Voltage values are with respect to network ground terminal.
6/ Based on extrapolation of 30 day Aging data using logarithmic curve fitting.
7/ Temperature limits are -45 ºC and +85 ºC
8/ Guaranteed by design, not tested. Range shall be sufficient to remove frequency drift that incurred during screening.
9/ Value shown is for supply voltage “A”; sensitivity shall be nominally -2 ppb/ohm and -40 ppm/volt for “L” supply voltage option.
10/ Guaranteed by design, not a screening limit.



NOTES:

1.) Dimensions are in inches.
2.) Lead numbers are for reference only and are not marked on the unit.
3.) A triangle symbol is marked on the corner of the package to indicate Pin 1.
4.) All pins with function NC and/or ITP may not be connected as external tie or connections.

PIN NO.	DESIGNATION
1 - 3	NC
4	External Frequency Adjust
5	Ground/Case
6 - 10	NC
11	VCC
12	Output
13	VCC
14 - 32	NC

FIGURE 1. PACKAGE DIMENSIONS AND TERMINAL CONNECTIONS